claim 2 is allowable at least for the reason claim 1 is allowable as well as for the features it recites.

Claim 5 is directed to a semiconductor device including a semiconductor chip, a wiring board joined to one surface of the semiconductor chip and electrically connected to the semiconductor chip and a warp preventing board joined to the other surface of the semiconductor chip and composed of the same material as that of the wiring board.

Claim 5 recites that the warp preventing board is another wiring board and another semiconductor chip is electrically connected to the warp preventing board being joined to a surface, facing away from the semiconductor chip, of the warp preventing board.

It is respectively submitted that the rejection is improper because the applied art fails to teach each element of claim 5, particularly a stacked structure of claim 5. Specifically, the applied art fails to teach that a warp preventing board is another wiring board and another semiconductor chip is electrically connected to the warp preventing board being joined to a surface, facing away from the semiconductor chip, of the warp preventing board. Thus, is respectfully submitted that claim 5 is allowable over the applied art.

Furthermore, the Office Action states that Shirai discloses "an external connection member (9) for surface mounting on the surface of the wiring board (1, 201) facing away from a semiconductor chip (210)." In the structure shown in Figures 6A-6F of Shirai, a circuit chip 210 is sandwiched by a pair of PET sheets 201 and 212. However, the PET sheet 201 as a base cannot be a wiring board as recited in claim 1. That is, a PET sheet cannot have an internal wiring that electrically connects an electronic component mounted on one surface thereof and an external connection electrode formed on the other surface thereof. Moreover, a PET sheet cannot have an external connection member on the surface thereof facing away from an electrical component.

The structure of the wiring board of the claimed invention is more particularly described in the specification on page 6, lines 4-16. For convenience of the Examiner,

an illustration labeled Exhibit 1 is attached hereto to assist in explaining the claimed invention.

The Office Action also refers to Figure 2 of Shirai. In this structure, a ceramic board is employed for a base board 1. The base board 1 is provided with conductor layers 8 via holes that penetrate the board 1, and the conductor layers 8 are connected to external interface pins 9. However, the conductor layers 8 just vertically penetrate the ceramic board 1 and do not correspond to internal wirings as formed in the wiring board of the claimed invention.

Furthermore, it is impossible to provide a via hole in a PET sheet to obtain a combined structure of Figures 2 and 6. Therefore, even a combination of the structures shown in Figures 2 and 6A-6F cannot render the claimed invention to be obvious to one of ordinary skill in the art.

With regard to claim 5, Shirai does not disclose that a PET sheet 212 provided above a circuit chip 210 is replaceable with a wiring board or that such wiring board is joined to an inactive surface of a semiconductor chip or that another semiconductor chip is joined to a surface of such wiring board.

Claim 2 is canceled and therefore the rejection as applied to claim 2 is now moot.

For at least the reasons discussed above, withdrawal of the rejection is respectfully requested.

Claim 3 is rejected under 35 U.S.C. 103(a) as unpatentable over Shirai et al. in view of Ball (U.S. Patent No. 6,165,815). The rejection is respectfully traversed.

Ball discloses, in Fig. 8 of his patent, a die assembly 800 that has a pair of substrates 606 and 808 which sandwich the chip-on-chip structure formed by a pair of dies 602 and 604 adhere to each other by a layer of an adhesive 618.

Claim 3 depends from claim 1 and includes all of the features of claim 1. Claim 3 is therefore allowable at least for the reason claim 1 is allowable as well as for the features it recites. Specifically, claim 3 recites that the warp preventing board is another wiring board and another semiconductor chip is electrically connected to the

warp preventing board being joined to a surface, facing away from the semiconductor chip, of the warp preventing board. In other words, the Ball patent fails to disclose that a circuit board is joined to an inactive surface of a semiconductor chip. Additionally, Shirai does not disclose that a PET sheet 212 provided above a circuit chip 210 is replaceable with a wiring board or that such wiring board is joined to an in active surface of a semiconductor chip or that another semiconductor chip is joined to a surface of such wiring board. For least these additional reasons, claim 3 is allowable over the applied art.

Withdrawal of the rejections is respectfully requested.

Claim 4 is rejected under 35 U.S.C. 103(a) as unpatentable over Shirai et al. in view of Lee (U.S. Patent No. 6,303,997). The rejection is respectfully traversed.

Lee discloses, in Fig. 1 of his patent, a stacked, laminated semiconductor package unit that has a plurality of individual packages 100' stacked on top of each other. Each of the semiconductor package 100' has a printed circuit board 2', a semiconductor chip 1' bonded to the top surface of the printed circuit board 2', and solder balls 4' provided in a peripheral area on the lower surface of the printed circuit board 2'.

Claim 4 depends from claim 1 and includes all of the features of claim 1. Thus, claim 4 is allowable at least for the reason claim 1 is allowable as well as for the features it recites. Specifically, claim 4 recites a wiring material for electrically connecting the wiring board and the warp preventing board is interposed therebetween. In other words, Lee, which fails to disclose a warp preventing board, discloses a stacked structure of a plurality of semiconductor packages. However, there is a gap between the inactive surface of the semiconductor chip 1' and a printed circuit board 2', so that the printed circuit board never has a function for preventing warp of the semiconductor package 100'. Thus, claim 4 is allowable over the applied art for this additional reason.

Withdrawal of the rejection is respectively requested.

In view of the foregoing, reconsideration of the application and allowance of the

pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Please charge any fee deficiency or credit any over payment to Deposit Account No.18-0013 that is necessary to consider an appropriate response timely filed.

Respectfully submitted,

Dated: January 9, 2003

By: _____
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Enclosure(s): Appendix I (Marked-Up Version of Amended Claim)
Petition for Extension of Time (two months)
Exhibit 1

DC109916

APPENDIX I

(MARKED-UP VERSION OF AMENDED CLAIMS)

1. (Amended) A semiconductor device comprising:

a semiconductor chip;

a wiring board joined to one surface of the semiconductor chip and electrically connected to the semiconductor chip, the wiring board having a wiring board thickness; and

a warp preventing board joined to the other surface of the semiconductor chip and composed of the same material as that of the wiring board, the warp preventing board having a warp preventing board thickness substantially equal to the wiring board thickness, wherein an external connection member for surface mounting is arranged on a surface, facing away from the semiconductor chip, of the wiring board.

Exhibit 1